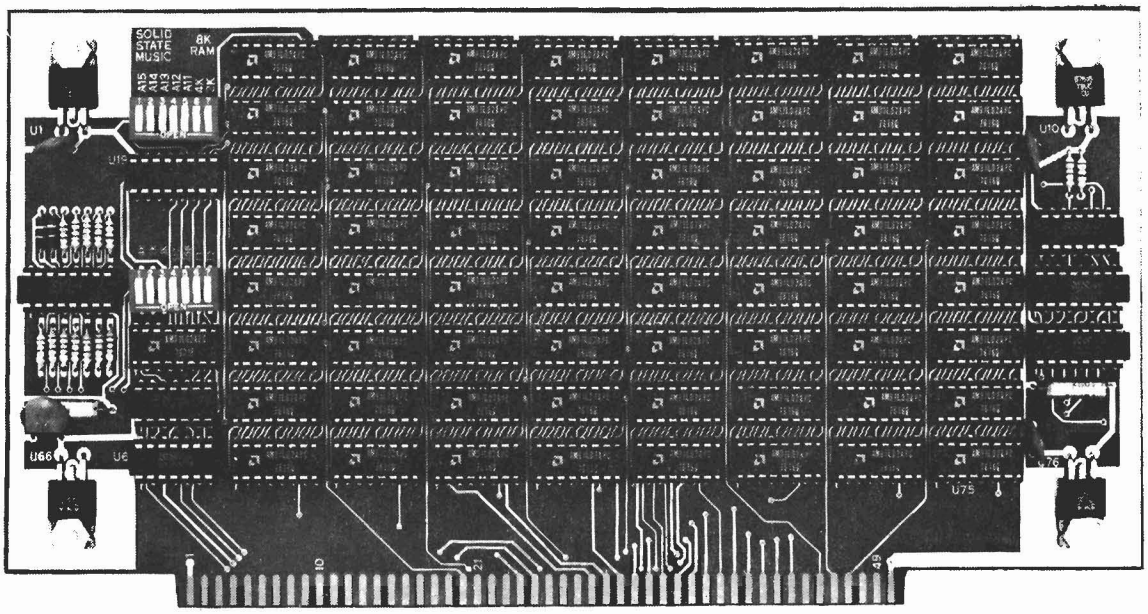
Solid State Music

MB6A

8K RAM BOARD



FEATURES

- Plug compatible with the ALTAIR 8800 and IMSAI 8080, or any other system using the "ALTAIR bus."
- Low-power, 500 nanosecond RAMs. No wait cycles required.
- Low-power Schottky support chips.
- DIP switch selection of memory address assignment and wait cycles.
- Memory protect can be set for increments of 256 bits, 512 bits, 1K, 2K, 4K or 8K by DIP switch.
- T.I. low profile sockets provided for all RAMs and ICs.
- Gold plated edge connector contacts.

PARTS LIST

1	PC Board with gold fingers
69	16 pin low-profile sockets
3	14 pin low-profile sockets
2	7 position DIP switches
65	91L02APC/D2102AL-4 low-power RAMs
1	74LS00
1	7402
1	74LS42
1	74LS74
2	74367 (DM 8097)
1	DM 8131
4	7805 or 340T-5 regulators
2	2.7 uF/ 20V tantalums
4	0.1 uF disc capacitors
14	2.7K ohm, ¼W resistors
2	39K, ¼W resistors
4	sets #6 screws, nuts and washers
1	instruction set

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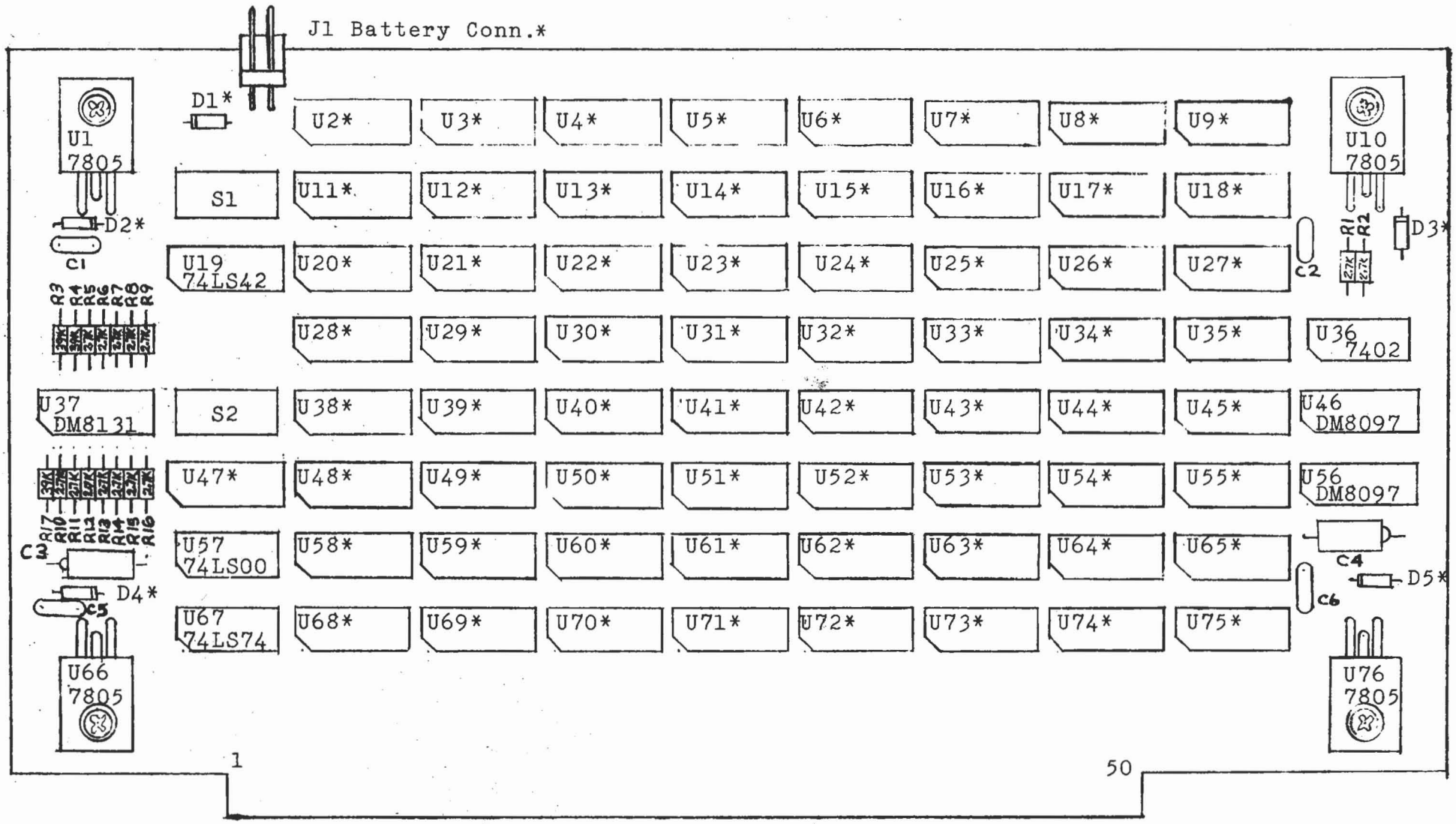

FIG 1

*NOTES: 1) All RAMs D2102AL-4 or AM91L02A
2) Caution: Observe position of cathode band-Failure to do so may cause damage
3) Vcc for battery back up should be 1.5 to 2.0 volts measured at pin 10 of the RAMs. Voltages HIGHER or LOWER may cause loss of data.
4) Add jpr 1 for SOL mainframes only.

ASSY DWG MB6A rev. 2

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MB6A- 8K STATIC MEMORY BOARD

1.0 ASSEMBLY INSTRUCTIONS (refer to Figure 1)

- [ ] Check kit contents against parts list.

- [ ] Check PC board for possible warpage and straighten if required.

- [ ] Insert 69 sixteen-pin sockets into the component side of the board with the "pin 1" index toward the ~~top~~ left of the board. (The component side is the side on which "Solid State Music" is printed.)

- [ ] Insert 3 fourteen-pin sockets. DON'T SOLDER!

- [ ] Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.

- [ ] Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the sockets pins are through the holes.)

  Note: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or steel wool.

- [ ] On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.

- [ ] Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on top while reheating each soldered pin.

- [ ] Complete soldering the remaining pins of each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron tip is recommended.

- [ ] Observing polarity, insert and solder the tantalum caps.

- [ ] Insert and solder the 4 disc capacitors.

- [ ] Insert DIP switches with the word "OPEN" toward the bottom of the board. Solder.

- [ ] Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending position to match the board holes--allow for a bend radius.

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1.0 ASSEMBLY (continued)

- [x] Bend regulator leads to match holes in board.
- [ ] If available, apply thermal compound to the back side of each regulator case (the part that lies flat against the board).
- [x] Drop regulators in place on front of board, insert #6 screws from front, and secure firmly with lock washer and nut.
- [x] Solder regulator leads to pads on back of board. Do not use excessive heat.
- [x] Insert and solder the 14 2.7K ohm and 3 39K ohm resistors. *
- [x] Insert and solder 5 diodes (observing polarity) and molex battery connector.
- [ ] Apply power (+8 volts approx.) to board by plugging into computer or by connection from a suitable power supply and measure the regulated output of each regulator. If less than 4.8 volts is measured (allowing for meter accuracy) check for shorts or wiring errors. CAUTION! WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGUALTORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS WHILE BEING TESTED. BETTER SAFE THAN SORRY - KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!
- [ ] Insert the following ICs in their sockets: U19, U36, U37, U46, U47 (a91L02APC), U56, U57, and U67. Be sure all pins are seated in the sockets. Repeat voltage checks.

2.0 FUNCTIONAL CHECK

WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

- [ ] Install the first 2K of 91L02As (U2 through U9 and U11 through U18). Be sure pins are seated in sockets.
- [ ] Set S1 as follows:

A11 and A12 -- open
A13 and A15 -- closed
2K and 4K -- open

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2.0 FUNCTIONAL CHECK (continued)

☐ Set S2 as follows:

4k, 2k, 1k, 512, 256, and T1 -- open
T2 -- closed

The above switch positions set the following conditions:

Address -- 0000-1FFF (000-000 through 037-377 octal)
Memory Complement -- 8K
Memory Protect Increment -- 8K
Memory Wait Cycles -- none

☐ Install board. Remember, this board, addressed per above setting, must have the first 8K uncontested. Any boards addressed for the first 8K positions must be readdressed or removed.

☐ "Examine" at octal 000 000, verify protect/unprotect conditions.

☐ "Examine" at octal 007 377, verify protect/unprotect conditions.

☐ Manually program with the front panel switches to verify that data can be stored. Don't forget to unprotect the memory before you do this.

☐ Repeat the above steps until all 8K have been verified as functional.

If you're set up to BASIC, it is an excellent dynamic test of your memory system. Be sure that all memory in the system has been unprotected.

3.0 SET-UP

3.1 ADDRESS SELECTION (S1)

	Address Range Hex	High Order Bits A15	A14	A13	A12	A11	DIP Switch Setting A15	A14	A13	A12	A11
8K	0000 - 1FFF	0	0	0	0	0	ON	ON	ON	ON	ON
16K	2000 - 3FFF	0	0	1	0	0	ON	ON	OFF	ON	ON
24K	4000 - 5FFF	0	1	0	0	0	ON	OFF	ON	ON	ON
32K	6000 - 7FFF	0	1	1	0	0	ON	OFF	OFF	ON	ON
40K	8000 - 9FFF	1	0	0	0	0	OFF	ON	ON	ON	ON
48K	A000 - BFFF	1	0	1	0	0	OFF	ON	OFF	ON	ON
56K	C000 - DFFF	1	1	0	0	0	OFF	OFF	ON	ON	ON
64K	E000 - FFFF	1	1	1	0	0	OFF	OFF	OFF	ON	ON

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3.0 SET-UP (continued)

3.2 MEMORY COMPLEMENT SELECTION

Memory Complement	DIP Switches 2K	4K
2K	ON	ON
4K	ON	OFF
8K	OFF	OFF

Note: The 2K switch activates address line A11
The 4K switch activates address line A12

3.3 MEMORY PROTECT INCREMENTS (S2)

Protect Increments	DIP Switch 256	512	1K	2K	4K
256	ON	ON	ON	ON	ON
512	OFF	ON	ON	ON	ON
1K	OFF	OFF	ON	ON	ON
2K	OFF	OFF	OFF	ON	ON
4K	OFF	OFF	OFF	OFF	ON
8K	OFF	OFF	OFF	OFF	OFF

Note: Switch arrangements other than those shown above provide other protect patterns.

3.4 MEMORY WAIT CYCLES

RAM Access Time	DIP Switch T1	T2	Wait Cycles
less than 550 ns	DONT CARE	ON	none
550ns to 1050ns	ON	OFF	1
1050ns to 1550ns	OFF	OFF	2

4.0 TROUBLE SHOOTING HINTS

a. Check for proper settings of DIP switches.

b. Verify that all ICs are in the correct sockets.

c. Visually inspect all ICs to be sure that leads are in the sockets and not bent under.

d. Verify that the output voltage of each regulator is within 4.7 to 5.3 volts.

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4.0 TROUBLE SHOOTING HINTS (continued)

e. Inspect back side of board for solder bridges, running a small sharp knife blade between traces that appear suspicious. A magnifying glass is a must for this.

f. Be sure all memory has been unprotected.*

g. If you can't protect/unprotect memory:
(1) recheck address settings
(2) check U36 (7402)

h. If you have an addressing problem:
(1) check U19 (74LS42) for addresses A10 thru A12.
(2) check U37 (DM8131) for addresses A13 thru A15.

i. If you have a problem with data output (consistent missing bits):
(1) check U46 (DM8097) for bits 0 through 3.
(2) check U56 (DM8097) for bits 4 through 7.
(3) check U36 (7402) for all bits.

j. If you have a wait cycle problem:
(1) check U57 (74LS00) and U67 (74LS74).

*NOTE (IMSAI & Poly users): If you have not incorporated a protect/unprotect feature into your mainframe, we recommend removing U47 (protect memory) of the MB6 to insure reliable operation, as the memory can come up protected when power is turned on (if U47 is not removed)

5.0 THEORY OF OPERATION

5.1 GENERAL

The MB6 is an 8K-byte (8K x 8 bit) random access memory featuring:

* Selectable address
* Memory protect in selectable increments (from ½K to 4K)
* Selectable memory wait cycles (from 0 to 2)
* Extra low-power, 500ns RAMs
* Low-power, Schottky support chips

The memory chips employed are AMD 91L02A or NEC 2102AL-4 1K x 1 bit, static RAMs. The RAM chips are organized in an 8 row x 8 column matrix. Each column corresponds to one bit of the memory word and contains 8K bits of memory.

5.0 THEORY OF OPERATION (continued)

5.2 DATA LINES

The data inputs (Di) of all the RAMs in each column are bussed together and connected to the 8 CPU output lines (DO Ø thru DO 7) and the data outputs (Do) are bussed together and connected to the 8 CPU input lines (DI Ø thru DI 7). The bussing of output lines is made possible by the tri-state outputs of the RAMs. These output lines are buffered by tri-state buffers.

5.3 ROW ADDRESSING

Address lines A10 thru A12 are decoded by U19, a 4 to 10 line decoder. The decoders' output enables one of 8 rows of RAMs by activating the chip select lines of all the RAMs in one row. (The fourth line of the decoder is used only as an overall memory enable line, and the last 2 outputs are unused.)

5.4 RAM CELL ADDRESS

The 10 address lines on each chip are all bussed together and are fed directly by address lines A0 thru A9. These lines select a particular bit in each of the 64 RAMs.

5.5 BOARD ADDRESS

Address lines A13 thru A15 select a particular 8K block of memory. The address of the MB6 is user selected by switches A13 thru A15. If the address on lines A13 thru A15 matches the preselected address of the board, comparator U37 enables protect memory U47 and decoder U19, and unlocks the SMEMR, SOUT, and SINP signals (through pin 15 of U46). NOTE* If only 2K or 4K of memory are being used, address lines A12 and A11 may be assigned to the address of the board as required by closing switches 4K and 2K. This enables address selection switches A12 &/or A11 as well.

5.6 MEMORY PROTECT

Only one row of the protect memory U47 is used to retain protect status for the board. If all S2 positions are open, a single bit in the memory determines protect status for all 8K of memory. Assuming the protect memory has been activated ($\overline{CS}$=0) by a correct memory address input to comparator U37, activating the protect (unprotect) line writes a 0 (1) into the protect memory. The output

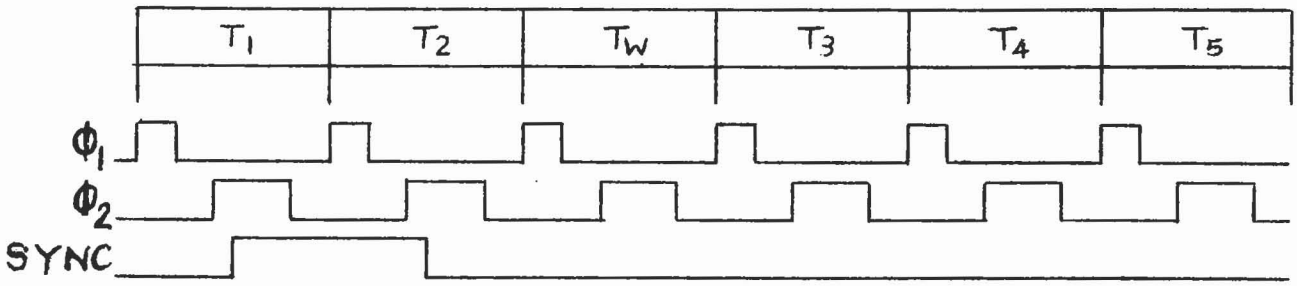
5.0 THEORY OF OPERATION (continued)

5.6 (continued)

is fed to a gate which disables (for protect) or enables (for unprotect) the MWRITE line. The output of the protect memory is also fed to a buffer whose output is the Protect Status ($\overline{PS}$) line.

Memory protect increments of less than 8K maybe selected by closing S2 positions as required; thereby assigning those address lines (A8 thru A12) desired to address various bits in the protect memory. In this way, protect increments from ½K to 4K maybe implemented.

5.7 CLOCK CIRCUITRY



Dual-D flip flop U67 is used to set the number of wait cycles the CPU goes through when reading or writing data on this board. It signals that it is ready to read or write by actuating the Ready line (PREADY).

Because 500ns RAMs are supplied with the MB6, no wait cycles are normally required. Therefore, T2 should be closed which clears the second DFF and maintains the Ready line in a high state.

If 1 wait cycle is desired, T2 should be open and T1 closed. This causes the output of DFF #1 to follow the SYNC pulse. Because its output is high until after the second Ø1 clock pulse in the Machine Cycle, the Ready line ($\overline{Q}$ of DFF #2) does not go high until after the third Ø2 clock pulse occurs. Therefore the third state in the machine cycle becomes a wait state. NOTE* The CPU looks for the Ready flag on the third Ø1 clock pulse of the Machine Cycle. If the Ready flag has not been raised, the CPU waits until the Ø1 clock and Ready flag occur concurrently.

If 2 wait cycles are desired, T1 & T2 should both be open. This causes Q of DFF #1 to go high at the start of SYNC, but it does not go low until the third Ø2 clock pulse occurs. Therefore, 2 Ø1 clock pulses are skipped before the Ready flag is raised

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5.0 THEORY OF OPERATION (continued)

5.8 MISCELLANEOUS FLAGS

The Memory Read line (SMEMR) is used to enable the tri-state buffers on the output lines. The Input (SINP) and Output (SOUT) lines are ORed together and the result is used to disable the flag output buffers ($\overline{PS}$ & PREADY flags) when the bus is being used for I/O.

6.0 WARRANTY

Parts guaranteed to original purchaser for 90 days, unless failure is due to misuse or failure of purchaser to excercise caution in assembly and operation. Registration card must be returned at time of purchase to validate warranty.

Assembled boards may be returned for service. A service charge will be made unless, in our judgement, the problem is due to a defective board or parts.

Our address: CYBERCOM/2102A Walsh Ave./ Santa Clara, Ca. 95050

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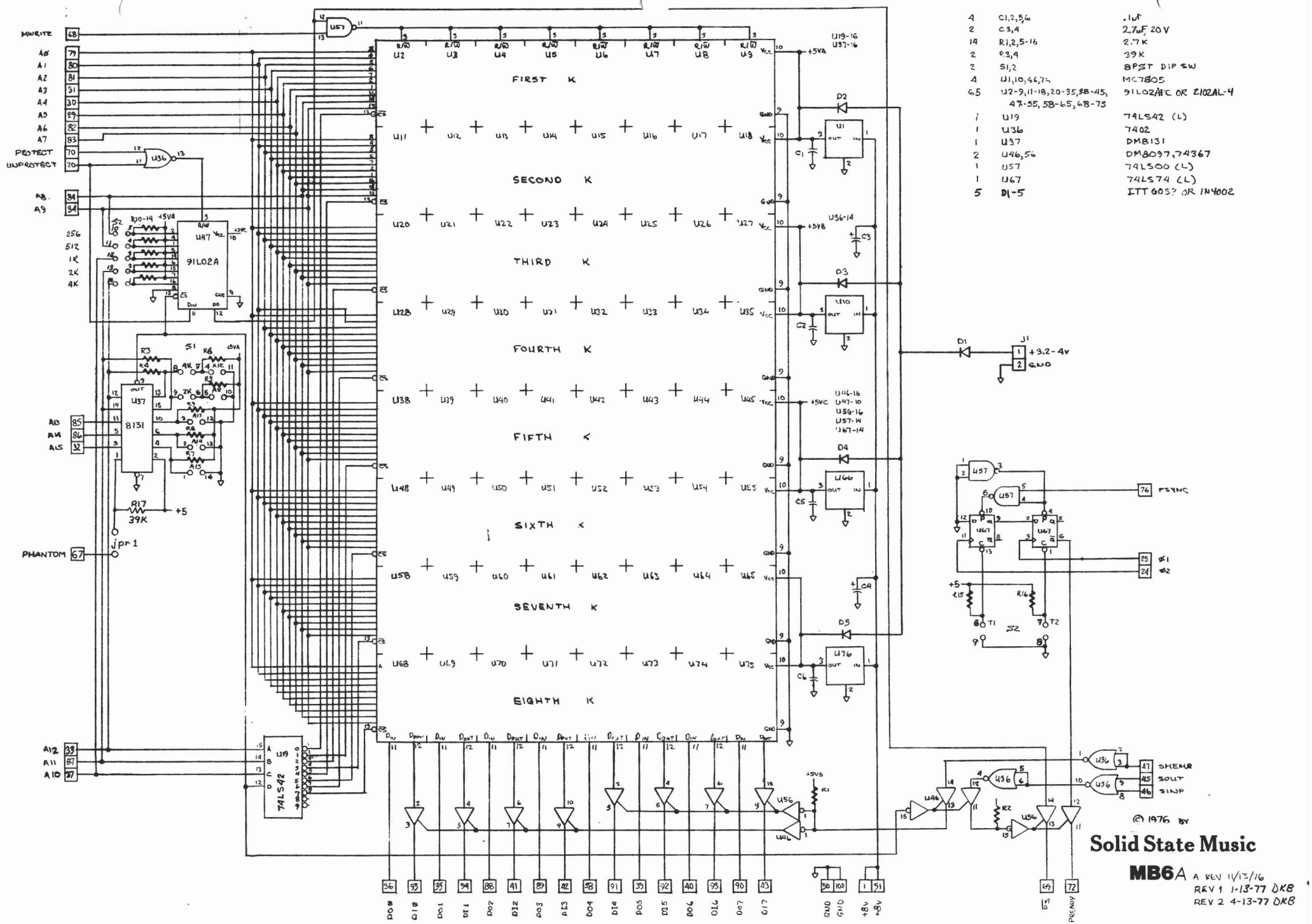
ADDENDUM FOR SOL USERS

SOL "PHANTOM"

The SOL system requires that the first block of memory is disabled for the first few machine cycles after power up in order to allow the monitor to initialize the system.

The RAM is disabled by means of the "Phantom" signal on pin 67 of the bus. This feature may be incorporated on the MB6 simply by adding jumper jpr 1.



4	C1,2,5,6	.1uF
2	C3,4	2.7uF 20V
14	R1,2,5-16	2.7K
2	R3,4	39K
2	S1,2	8PST DIP SW
4	U1,10,46,76	MC7805
65	U2-9,11-18,20-35,38-45, 47-55,58-65,68-75	91L02APC OR Z102AL-4
1	U19	74LS42 (L)
1	U36	7402
1	U37	DM8131
2	U46,56	DM8097,74367
1	U57	74LS00 (L)
1	U67	74LS74 (L)
5	D1-5	ITT 6052 OR IN4002